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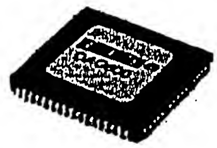


DAC600

DEMO BOARD AVAILABLE

12-Bit 256MHz Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION
- 256MHz UPDATE RATE
- –73dB HARMONIC DISTORTION AT 10MHz
- LASER TRIMMED ACCURACY: 1/2LSB
- –5.2V SINGLE POWER SUPPLY
- EDGE-TRIGGERED LATCH
- LOW GLITCH: 5.6pVs
- WIDEBAND MULTIPLYING REFERENCE INPUT
- 50Ω OUTPUT IMPEDANCE

APPLICATIONS

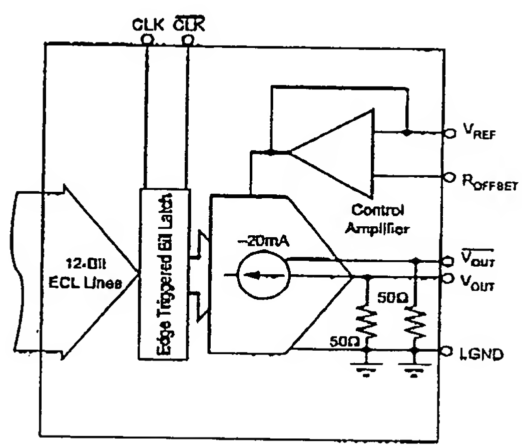
- DIRECT DIGITAL SYNTHESIS
- ARBITRARY WAVEFORM GENERATION
- HIGH RESOLUTION GRAPHICS
- COMMUNICATIONS LOCAL OSCILLATORS
  Spread Spectrum/Frequency Hopping
  Base Stations
  Digitally Tuned Receivers

DESCRIPTION

The DAC600 is a monolithic, high performance digital-to-analog converter for high frequency waveform generation. The internal segmentation and latching minimize output glitch energy and maximizes AC performance. Resistor laser trimming provides for excellent DC linearity.

The ECL compatibility provides for low digital noise at high update rates. The complementary 50Ω outputs and low output capacitance simplifies transmission line design and filtering at the output.

The DAC600 combines precision thin film and bipolar technology to create a high performance, cost effective solution for modern waveform synthesis.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

 PDS-1153E Printed in U.S.A. November, 1996

SPECIFICATIONS

ELECTRICAL

At +25°C V_{REF} = +1.0V, V_{EEA} = V_{EED} = –5.2V, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	DAC600AN MIN	DAC600AN TYP	DAC600AN MAX	DAC600BN MIN	DAC600BN TYP	DAC600BN MAX	UNITS
DIGITAL INPUTS									
Logic	12 Parallel Input Lines, ECL								
Resolution					12			*	Bits
ECL Logic Input Levels: V_{IL}	Logic "0"	Full	–1.48	–1.85	–2	*	*	*	V
I_{IL}		Full			2			*	µA
V_{IH}	Logic "1"	Full	–1.1	–0.75	0	*	*	*	V
I_{IH}		Full			200			*	µA
DIGITAL TIMING									
Input Data Rate		Full	DC		256	*		*	MHz
CLK Pulse Width High or Low		Full	1.95			*			ns
Set-up Time		Full	1.5	1.0		*	*		ns
Hold Time (Referred to CLK)		Full	1.9	1.7		*	*		ns
Propagation Delay		Full		2			*		ns
ANALOG OUTPUT									
Bipolar Output Current	R_L = 0Ω	Full	19	20	21	*	*	*	mA
Output Resistance		Full	47.5	50	52.5	49	*	51	Ω
Output Capacitance		Full		15			*		pF
CONTROL AMPLIFIER									
Input Resistance		Full		800			*		Ω
Full Power Bandwidth	–3dB	Full		10			*		MHz
Offset		+25°C		0	±1		0	±0.5	mV
Input Reference Range		Full	100mV		±1.25	*		*	V
TRANSFER CHARACTERISTICS									
Integral Linearity Error(1): $V_{OUT\ NOT}$	Best Fit Straight Line	+25°C		±0.012	±0.024		±0.006	±0.012	%FSR
$V_{OUT\ NOT}$		Full		±0.024	±0.036		±0.012	±0.024	%FSR
V_{OUT}		+25°C			±0.1			±0.1	%FSR
Differential Linearity Error(1): $V_{OUT\ NOT}$		+25°C			±0.024			±0.012	%FSR
$V_{OUT\ NOT}$		Full			±0.038			±0.024	%FSR
V_{OUT}		+25°C			±0.1%			±0.1%	%FSR
12-Bit Monotonicity		+25°C		Guaranteed			Guaranteed		
		Full		Typical			Guaranteed		
Output Offset Current: $V_{OUT\ NOT}$	Bits 1-12 HIGH	+25°C		75	150		50	100	µA
$V_{OUT\ NOT}$		Full		57	150		50	100	µA
Gain Error(2)		+25°C		±0.5	±1.5		±0.5	±1.0	%
		Full		±1.3	±2.0		±1.1	±2.0	%
Output Leakage Current	V_{REF} = 0V, Bits 1-12 LOW, $V_{OUT\ NOT}$	+25°C		10	75		5	50	µA
TIME DOMAIN PERFORMANCE									
Glitch Energy	Major Carry	+25°C		5.6			*		pVs
Fall Time	90% to 10%	+25°C		510			*		ps
Rise Time	10% to 90%	+25°C		770			*		ps
Settling Time(3)									
±0.1% FSR	Major Carry, 1 LSB Change	Full		4			*		ns
±0.024% FSR		Full		15			*		ns
DYNAMIC PERFORMANCE									
Spurious Free Dynamic Range (4)									
f_O = 1MHz	f_{CLOCK} = 50MHz	+25°C		74		70	77		dBFS(3)
f_O = 10MHz	f_{CLOCK} = 50MHz	+25°C		71		64	73		dBFS
f_O = 1MHz	f_{CLOCK} = 100MHz	+25°C		72		70	75		dBFS
f_O = 10MHz	f_{CLOCK} = 100MHz	+25°C		68		66	70		dBFS
f_O = 20MHz	f_{CLOCK} = 100MHz	+25°C		61		58	62		dBFS
f_O = 10MHz	f_{CLOCK} = 200MHz	+25°C		66		66	70		dBFS
f_O = 20MHz	f_{CLOCK} = 200MHz	+25°C		58		62	67		dBFS
f_O = 50MHz	f_{CLOCK} = 200MHz	+25°C		52		50	55		dBFS
Output Noise	Bits 1-12 HIGH	+25°C		10.6			*		$nV/\sqrt{Hz}$
POWER SUPPLIES									
Supply Voltages: V_{EE}		Full	–4.5	–5.2	–5.5	*	*	*	V
Supply Currents: I_{EEA}	Pins 33 and 34	Full	30	48	80	*	*	*	mA
I_{EED}	Pins 5 and 55	Full	110	150	190	*	*	*	mA
Power Consumption	Operating	Full		800mW	1.3		*	*	W
TEMPERATURE RANGE									
Specification: DAC600AN, BN	Ambient	Full	–40		+85	*		*	°C
θ_{JA}				30			*		°C/W

* Same as specification for DAC600AN.

NOTES: (1) Linearity tests are measured into a virtual ground (op amp). (2) Gain error in % is calculated by: $GE(\%) = \frac{V_{MEASURED}(FS) - V_{IDEAL}(FS) \times 100}{V_{IDEAL}(FS)}$ (3) Settling time is influenced by the load due to fast edge speeds. Use good transmission line techniques for best results. (4) Spurious free dynamic range is measured from the fundamental frequency to any harmonic or non-harmonic spurs within the bandwidth $f_{CLK}/2$, unless otherwise specified.

ORDERING INFORMATION

PRODUCT	DESCRIPTION	TEMPERATURE RANGE (AMBIENT)
DAC600AN, BN	68-Pin Plastic QUAD	–40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

V_{EEA}	0.3 to –7
V_{EED}	0.3 to –7
Logic Inputs	0 to –5.5V
Reference Input Voltage	0 to +1.25V
Reference Input Current	0 to 1.56mA
Case Temperature	–40°C to +125°C
Junction Temperature	+150°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC600AN, BN	68-Pin Plastic QUAD	312-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

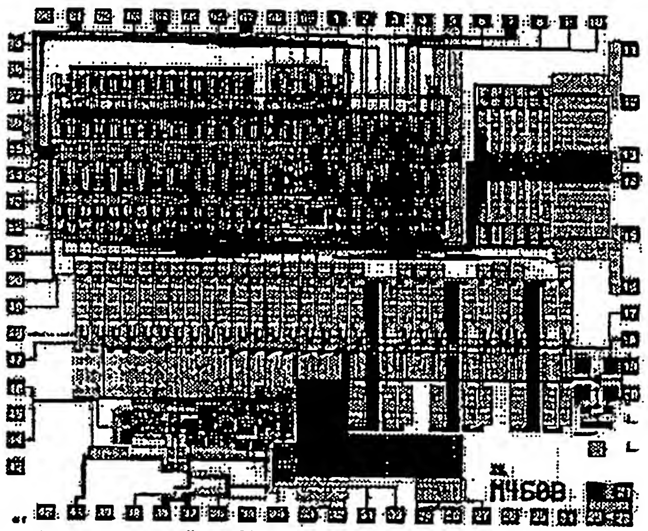
PIN DEFINITIONS

PIN #	DESIGNATION	DESCRIPTION	PIN #	DESIGNATION	DESCRIPTION
1	BYPASS	Disables Latching of Data	35	$V_{REF/2}$	Analog Reference Voltage Center Tap
2	CLK	CLOCK	36	NC	
3	CLKNOT	CLOCKNOT	37	NC	
4	DGND	Digital Ground	38	V_{REF}	Analog Reference Voltage
5	DV_{EE}[1]	–5.2V Supply	39	V_{REF}	Analog Reference Voltage
6	Bit 9		40	NC	
7	Bit 10		41	NC	
8	Bit 11		42	R_{OFFSET}	Offset Compensation
9	Bit 12	LSB	43	NC	
10	NC		44	BYPASS	0.1µF Bypass to Ground
11	NC		45	NC	
12	NC		46	NC	
13	V_{OUT}	DAC Output	47	ALTCOMPC	Control Amp PTAT Reference Compensation[2]
14	V_{OUT}	DAC Output	48	AGND	Analog Signal Ground
15	LGND	Ladder Ground	49	NC	
16	LGND	Ladder Ground	50	LBIAS	Ladder Bias Alternate Compensation[2]
17	V_{OUTNOT}	DAC Output Complement	51	NC	
18	V_{OUTNOT}	DAC Output Complement	52	NC	
19	NC		53	NC	
20	AGND	Analog Ground	54	Bit 1	MSB
21	NC		55	DV_{EE}	Digital –5.2V Supply
22	NC		56	DGND	Digital Signal Ground
23	NC		57	DGND	Digital Signal Ground
24	NC		58	Bit 2	
25	NC		59	Bit 3	
26	BYPASS	0.1µF Bypass to Ground	60	Bit 4	
27	NC		61	NC	
28	ALTCOMPIB	PTAT-IB Reference Compensation[2]	62	Bit 5	
29	AGND	Analog Ground	63	DGND	Digital Ground
30	AGND	Analog Ground	64	Bit 6	
31	NC		65	Bit 7	
32	LOOPCRNT	DAC Reference Alt. Loop Current (Connect to AGND)	66	DGND	Digital Ground
33	V_{EE}[1]	–5.2V Supply	67	Bit 8	
34	V_{EE}[1]	–5.2V Supply	68	NC	

NC: no connect

NOTE: (1) Pins 5 and 55 typically draw 150mA of current. Pins 33 and 34 combined typically draw 46mA. (2) Connect bypass capacitor to V_{EE}.

DICE INFORMATION



DAC600 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bypass	36	NC
2	CLK	37	V_{REF}
3	CLKNOT	38	V_{REF}
4	DGND	39	NC
5	DV_{EE}	40	NC
6	Bit 9	41	R_{Offset}
7	NC	42	NC
8	Bit 10	43	NC
9	Bit 11	44	NC
10	Bit 12	45	NC
11	V_{OUT}	46	ALTCOMPC
12	V_{OUT}	47	AGND
13	LGND	48	NC
14	LGND	49	LBIAS
15	V_{OUTNOT}	50	NC
16	V_{OUTNOT}	51	NC
17	NC	52	NC
18	AGND	53	Bit 1 (MSB)
19	NC	54	DV_{EE}
20	NC	55	DGND
21	NC	56	DGND
22	NC	57	Bit 2
23	NC	58	Bit 3
24	NC	59	Bit 4
25	NC	60	NC
26	NC	61	NC
27	ALTCOMPIB	62	NC
28	AGND	63	Bit 5
29	AGND	64	DGND
30	NC	65	Bit 6
31	LOOPCRNT	66	Bit 7
32	AV_{EE}	67	DGND
33	AV_{CC}	68	Bit 8
34	V_{REF2}	69	NC
35	NC		

Substrate Bias: Negative Supply $-V_{CC}$.
NC = Do not connect.

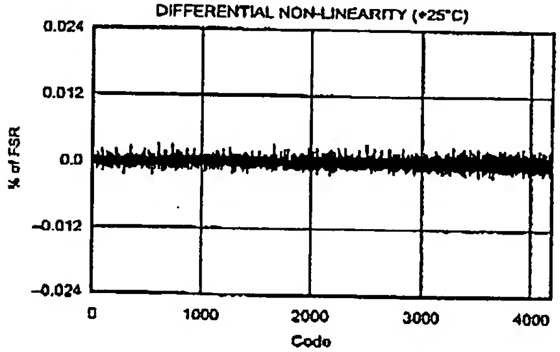
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	160 x 140 ±5	4.06 x 3.56 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	
Metallization	Gold	

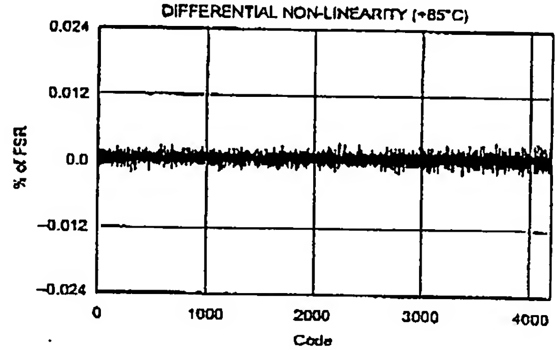
TYPICAL PERFORMANCE CURVES

At T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\ NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

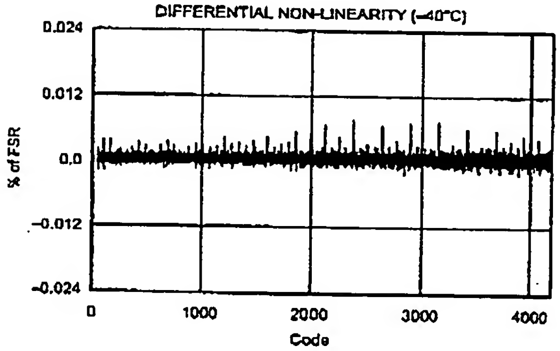
DIFFERENTIAL NON-LINEARITY (+25°C)



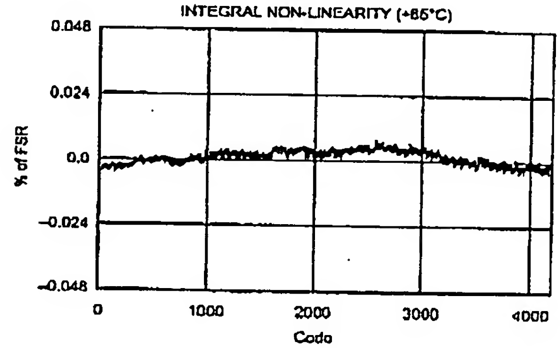
DIFFERENTIAL NON-LINEARITY (+85°C)



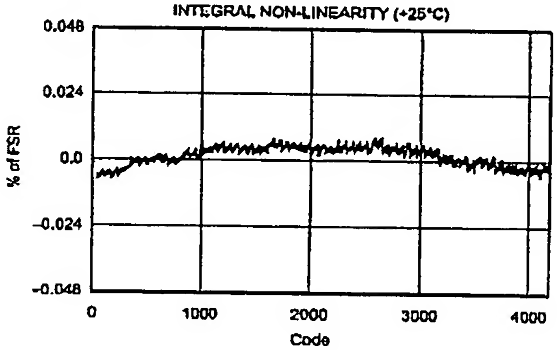
DIFFERENTIAL NON-LINEARITY (–40°C)



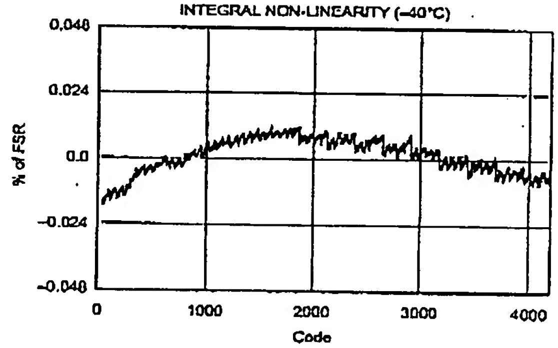
INTEGRAL NON-LINEARITY (+85°C)



INTEGRAL NON-LINEARITY (+25°C)



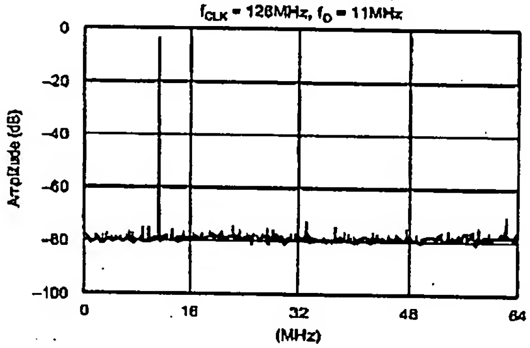
INTEGRAL NON-LINEARITY (–40°C)



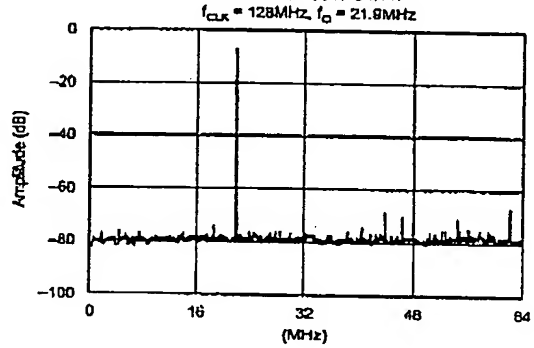
TYPICAL PERFORMANCE CURVES (CONT)

At T_{CASE} = +25°C, V_{REF} = +1.0V, measured at V_{OUTNOT}. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

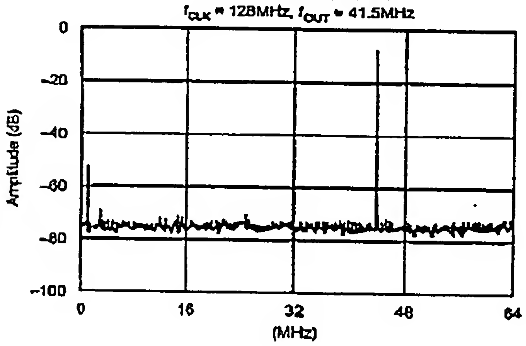
OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_O = 11MHz



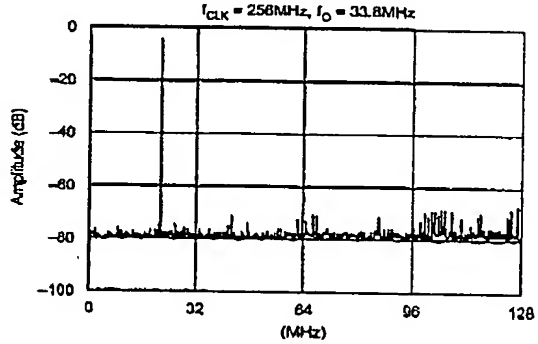
OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_O = 21.9MHz



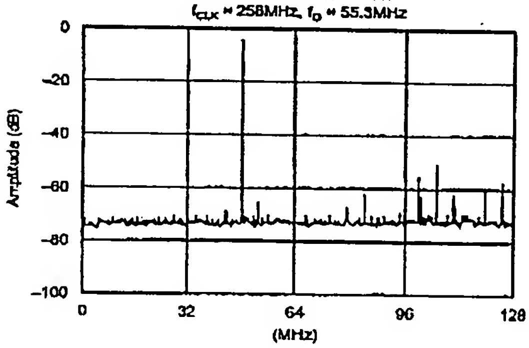
OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_{OUT} = 41.5MHz



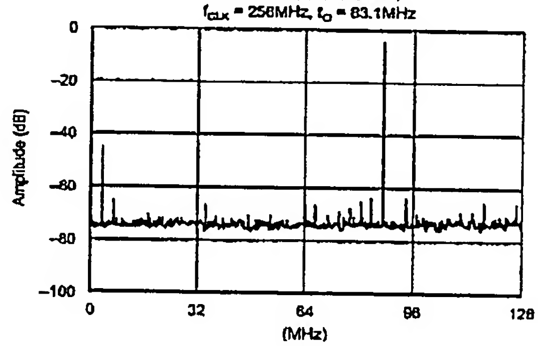
OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 33.8MHz



OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 55.3MHz



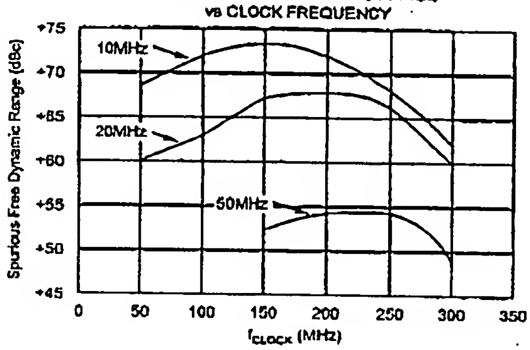
OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 83.1MHz



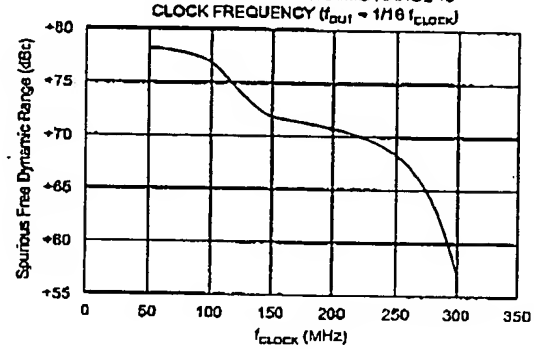
TYPICAL PERFORMANCE CURVES (CONT)

At T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\ NO1}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

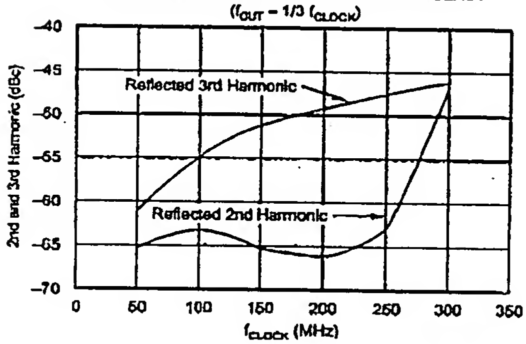
SPURIOUS FREE DYNAMIC RANGE vs CLOCK FREQUENCY



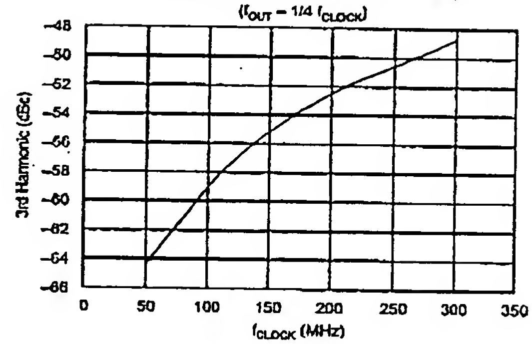
SPURIOUS FREE DYNAMIC RANGE vs CLOCK FREQUENCY (f_{OUT} = 1/16 f_{CLOCK})



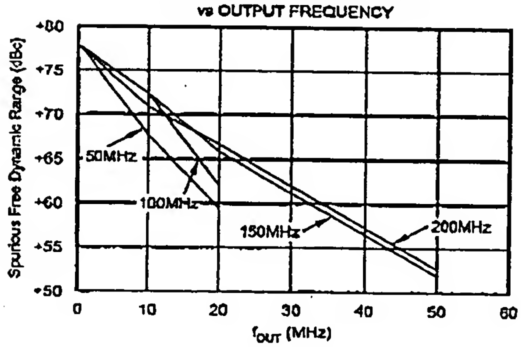
HARMONIC DISTORTION vs CLOCK FREQUENCY (f_{OUT} = 1/3 f_{CLOCK})



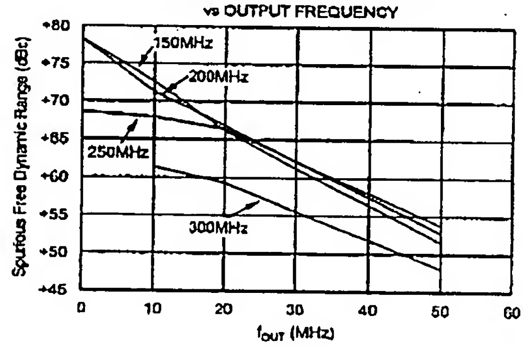
3RD HARMONIC vs CLOCK FREQUENCY (f_{OUT} = 1/4 f_{CLOCK})



SPURIOUS FREE DYNAMIC RANGE vs OUTPUT FREQUENCY



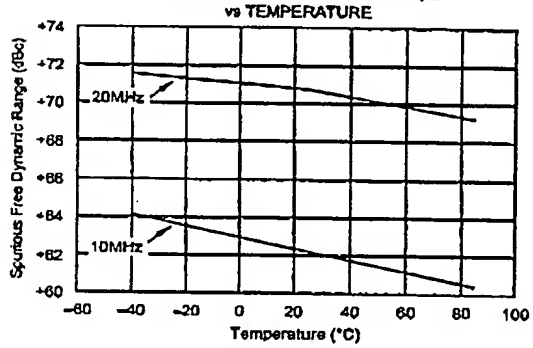
SPURIOUS FREE DYNAMIC RANGE vs OUTPUT FREQUENCY



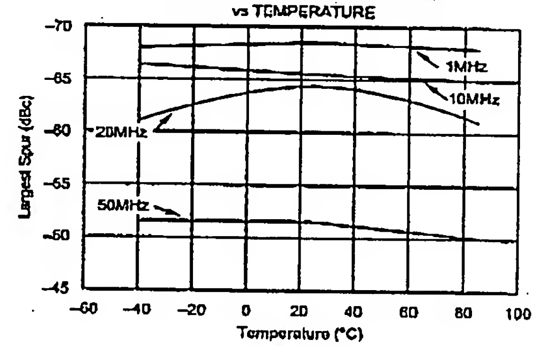
TYPICAL PERFORMANCE CURVES (CONT)

At T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\ NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

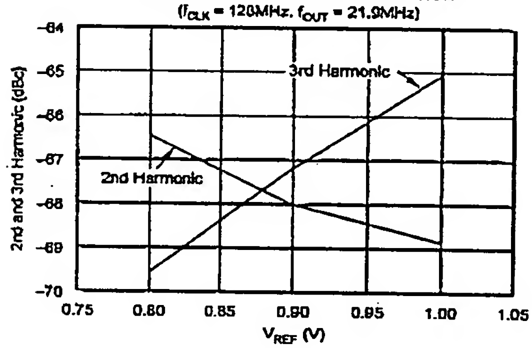
SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE



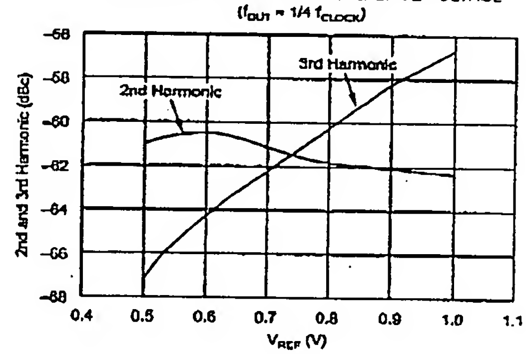
SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE



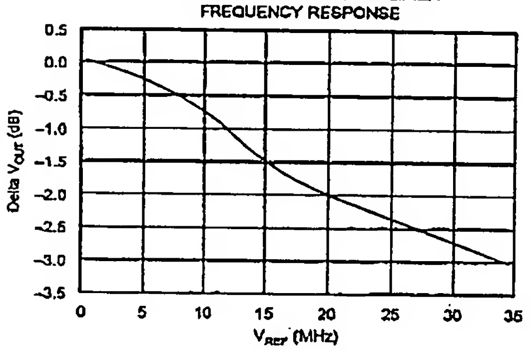
REFERENCE VOLTAGE vs DISTORTION
(f_{CLK} = 120MHz, f_{OUT} = 21.9MHz)



HARMONIC DISTORTION vs REFERENCE VOLTAGE
(f_{OUT} = 1/4 f_{CLOCK})

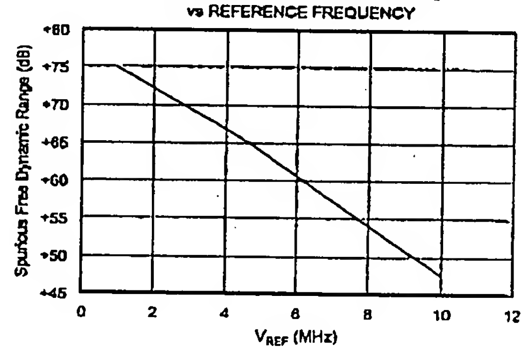


REFERENCE CONTROL AMPLIFIER FREQUENCY RESPONSE



V_{REF} Amplitude +0.75V DC 100mVp-p AC
(All Bits on, 47pF Pin 35)

SPURIOUS FREE DYNAMIC RANGE vs REFERENCE FREQUENCY



V_{REF} Amplitude +0.75V DC 100mVp-p AC
(All Bits on, 47pF Pin 35)

THEORY OF OPERATION

The DAC600 employs a familiar architecture where input bits switch on the appropriate current sources (Figure 1.) Bits 1-4 are decoded into 15 segments after the first set of latches. The edge triggered master-slave latches are driven by an internal clock buffer. Current sources for bits 5 and 6 are scaled down in binary fashion. These current sources are switched directly to the output of the R-2R ladder. Bits 7-12 are properly scaled and fed to the laser trimmed R-2R ladder.

Decoding of bits 1-4 into 15 segments and synchronizing the data with a master/slave register reduces glitching. If the BYPASS input is low, data is transferred to the output on the positive going edge of the clock. If BYPASS is high, data is transferred to the output regardless of clock state. All digital inputs are ECL compatible.

The output current sees 50Ω of output impedance from the equivalent resistance of a R-2R ladder. With all of the current sources off, the output voltage is at 0V. With all current sources on (–20mA), the output voltage is at –1V. Transfer function information is given in Tables I and II.

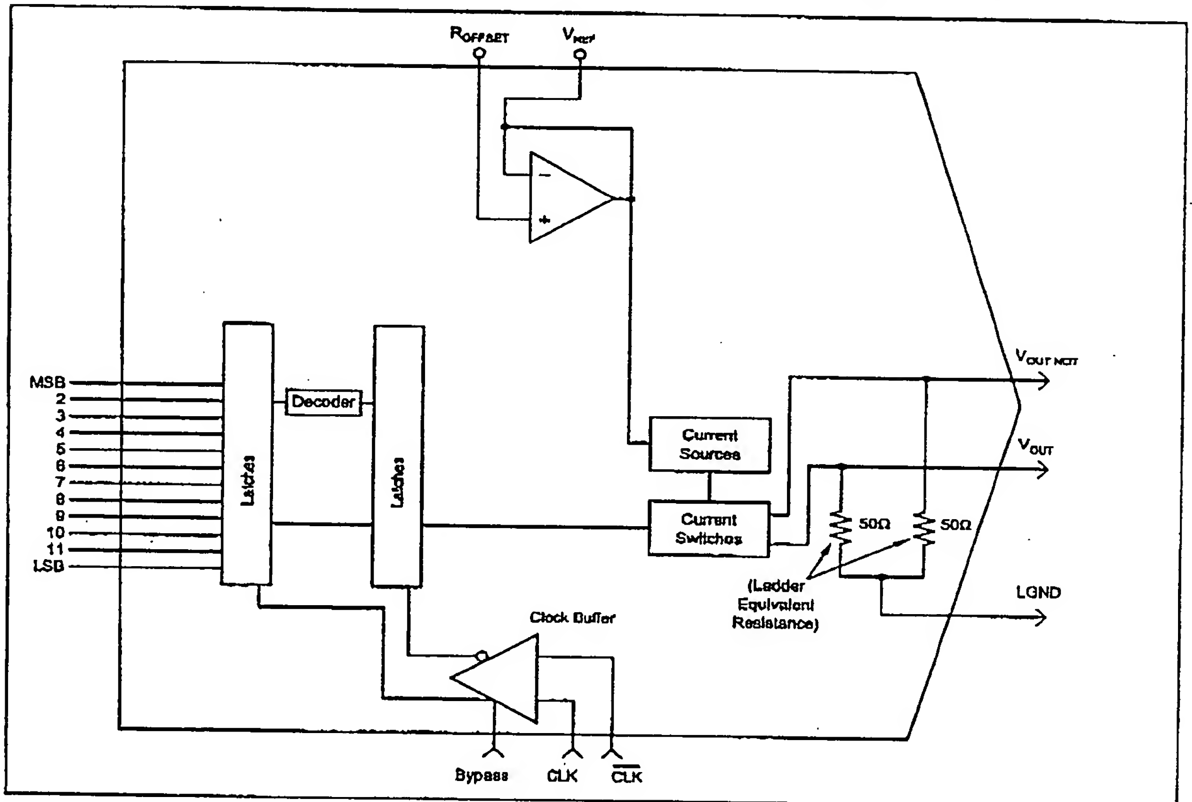


FIGURE 1. Basic DAC600 Architecture.

INPUT BITS 1 2 3 4 5 6 7 8 9 10 11 12	OUTPUT VOLTAGES V_{OUT}	NV_{OUT}
0 0 0 0 0 0 0 0 0 0 0 0	0V	–0.999756V
0 0 0 0 0 0 0 0 0 0 0 1	–244µV	0.999512V
•	•	
•	•	
•	•	
•	•	
1 0 0 0 0 0 0 0 0 0 0 0	–0.5	–0.499756
1 1 1 1 1 1 1 1 1 1 1 1	–0.999756V	0

TABLE I. Input Code vs Output Voltage Relationships.

BIT	VOLTAGE (No External Load, V_{OUT})
1	–0.5
2	–0.25
3	–0.125
4	–62.5mV
5	–31.25mV
6	–15.625mV
7	–7.8125mV
8	–3.9063mV
9	–1.9531mV
10	–976µV
11	–488µV
12 (LSB)	–244µV

TABLE II. Nominal Bit Weight Values.

There is also a complementary $V_{OUT\ NOT}$ output that allows for a differential output signal. The full scale complementary outputs (V_{OUT} and $V_{OUT\ NOT}$) can be simply modeled as –20mA in parallel with 50Ω. This gives an output swing of 0.5Vp-p with an external 50Ω load.

REFERENCE/GAIN ADJUSTMENT

The V_{REF} pin should be supplied by a +1.0V reference that is capable of supplying a nominal current of 1.25mA. An alternative would be the use of a 1.25mA current source. A low drift reference will minimize gain drift. A recommended reference circuit is given in Figure 2 as shown in the Typical Performance Curves, lowering the reference voltage to +0.8V will typically improve the Spurious Free Dynamic Range by a few dB.

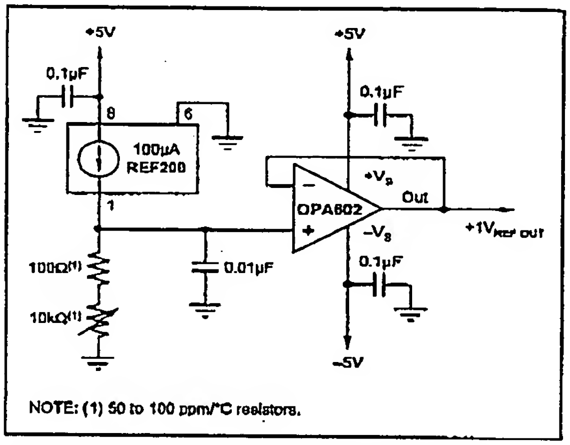


FIGURE 2. A Low Drift External Reference Circuit.

A low-cost alternative reference circuit is shown in Figure 3. This circuit uses the Burr-Brown REF1004-2.5 micropower voltage reference. Gain drift is dependent upon the temperature coefficient of the 1.2kΩ resistor. A TC of < 10ppm/°C is recommended.

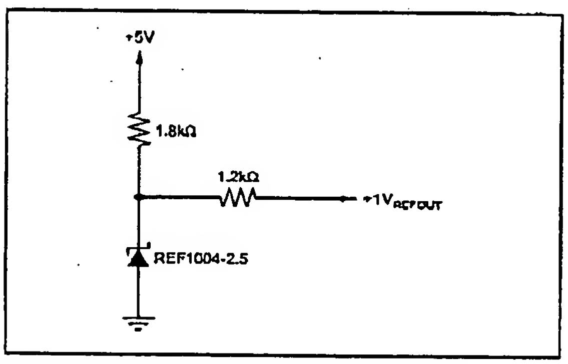


FIGURE 3. Low Cost External Reference Circuit.

The DAC600 can also accept a wideband multiplying reference input. The full power bandwidth of this reference is approximately 30MHz. Care must be taken not to exceed the minimum and maximum input reference voltage levels which are 100mV and +1.25V respectively (refer to the absolute maximum ratings section). In the multiplying reference mode, the 0.4µF bypass capacitor on LBIAS and the 0.1µF on pin 35 need to be removed. A 47pF capacitor to ground needs to be connected to pin 35 (Figure 4.)

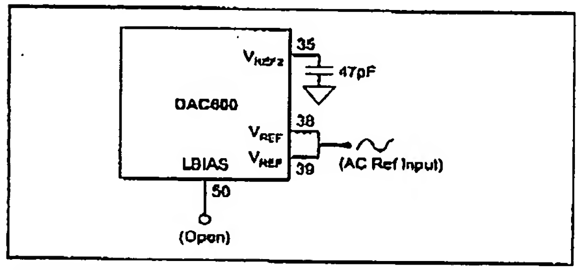


FIGURE 4. Connections for a Multiplying Reference Input.

TIMING

The DAC600 has an internal latch that is triggered on the rising edge of the clock when the BYPASS pin is set LOW. This master-slave mode of operation will assure that the 12 bits will arrive at the current sources with a minimum of data skew. Therefore, this mode is recommended for the vast majority of applications. Observing the minimum set-up and hold time recommendations will ensure proper data latching, refer to Figure 5 for complete timing specifications.

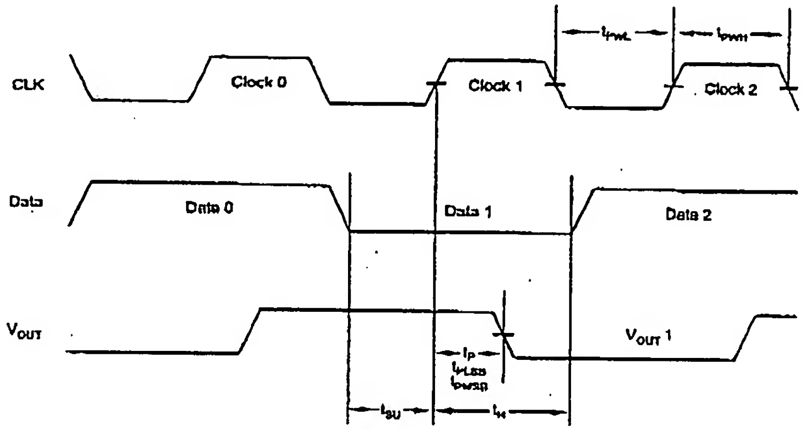
When BYPASS is set HIGH, the DAC600 will operate in the transparent mode. In this mode, both the master and slave registers are transparent and changes in input data ripple directly to the output. Since the four MSBs have a decoder delay, these bits arrive at the output approximately 600 picoseconds later than the lower 8 LSBs. Because this data skew causes glitch, this mode is not recommended for optimum AC performance.

The DAC600 has a differential ECL clock input. This clock input can also be driven by a single ended clock if desired by tying the CLKNOT input to an external voltage of –1.3V. Using a differential clock provides much improved digital feedthrough immunity, however.

DRIVING THE DAC600

The DAC600 inputs will most likely be driven by high speed ECL gate outputs. These outputs should be terminated using standard high speed transmission line techniques. Consult an ECL handbook for proper methods of termination.

Termination resistors should not be connected to the analog ground plane close to the DAC600. The fast changing digital bit currents will cause noise in the analog ground plane under this layout scheme. These fast changing digital currents should be steered away from the sensitive DAC600



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagation delay. 50% of CLK to 50% of V_{OUT}.		2		ns
t_{SU}	Setup time DATA must remain stable before CLK.	1.5	1.0		ps
t_H	Hold time DATA must remain stable after CLK.	1.9	1.7		ns
t_{PWL}	CLK pulse width low (50% to 50%).	1.95			ns
t_{PWH}	CLK pulse width high (50% to 50%).	1.95			ns
t_{PMSB}	Propagation delay, MSBs, transparent mode only.		2.1		ns
t_{PLSB}	Propagation delay, LSBs, transparent mode only.		1.5		ns

FIGURE 5. Timing Diagram.

analog ground plane. For speeds of up to 256MHz, series termination with 47Ω resistors will be adequate (Figure 6). This termination technique will greatly lessen the issue of termination currents coupling into the analog ground plane. This is shown in the typical DAC600 connection diagram (Figure 7.)

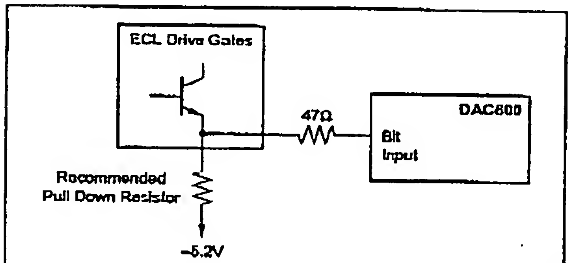


FIGURE 6. Series Bit Termination.

LAYOUT AND POWER SUPPLIES

A multilayer PC board with a solid ground and power planes is recommended. All of the ground pins (both analog and digital) should be connected directly to the analog ground plane at the DAC600.

Wide busses for the power paths are recommended as good general practice. External bypassing is recommended. A 10µF ceramic capacitor in parallel with a 0.01µF chip capacitor will be sufficient in most applications.

ALTCOMPB and ALTCOMPC should be bypassed with 0.1µF capacitors connected to V_{EEA}. When not used in the multiplying mode LBIAS should be bypassed with a 0.4µF capacitor connected to V_{EEA}. The heat spreader (pins 26 and 44) should be bypassed with a 0.1µF capacitor.

MAXIMIZING PERFORMANCE

In addition to optimizing the layout and ground of the DAC600, there are other important issues to consider when optimizing the performance of this DAC in various AC applications.

The DAC600 includes an internal 50Ω output impedance to simplify output interfacing to a 50Ω load. Because some loads may be a complex impedance, care must be taken to match the output impedance with the load. Mismatching of impedances can cause reflections which will affect the measured AC performance parameters such as settling time, harmonic distortion, rise/fall times, etc. Often complex impedances can be matched by placing a variable 3 to 10pF capacitor at the output of the DAC to ground. Also, probing the output of the DAC can present a complex impedance.

The typical performance curves of Spurious Free Dynamic Range vs various combinations of clock rate and/or input frequency should give a general idea of the spectral performance of the DAC under system specific clock and output frequencies. For variable frequency DDS and ARB applications, having a programmable frequency bandpass (smart) filter at the output of the DAC can greatly improve system

spur and noise performance by filtering out unwanted spur and noise spectra. Even with a programmable bandpass filter, care should be taken to update the DAC at greater than 4 times per cycle to (1) minimize the 2nd and 3rd harmonic magnitudes by having the output slew excessively between any successive clock and (3) to keep the 2nd harmonic and other even order harmonics from folding back close to the fundamental under the condition $f_{OUT} \approx 1/3\ f_{CLK}$ and (3) to keep the 3rd harmonic and other harmonics from folding back close to the fundamental under the condition $f_{OUT} = 1/4\ f_{CLK}$. The making use of the high update rate of the DAC600 helps to lessen the problems of large harmonics "folding back" into the passband.

For DDS applications, often the DAC itself is the limit in Spurious Free Dynamic Range (SFDR) performance. However, due to the high linearity of the DAC600, low frequency spurious performance may be limited by the digital truncation error of the phase accumulator/ROM combination. Most vendors supplying a combination of phase accumulator and ROM specify the SFDR of their digital algorithm.

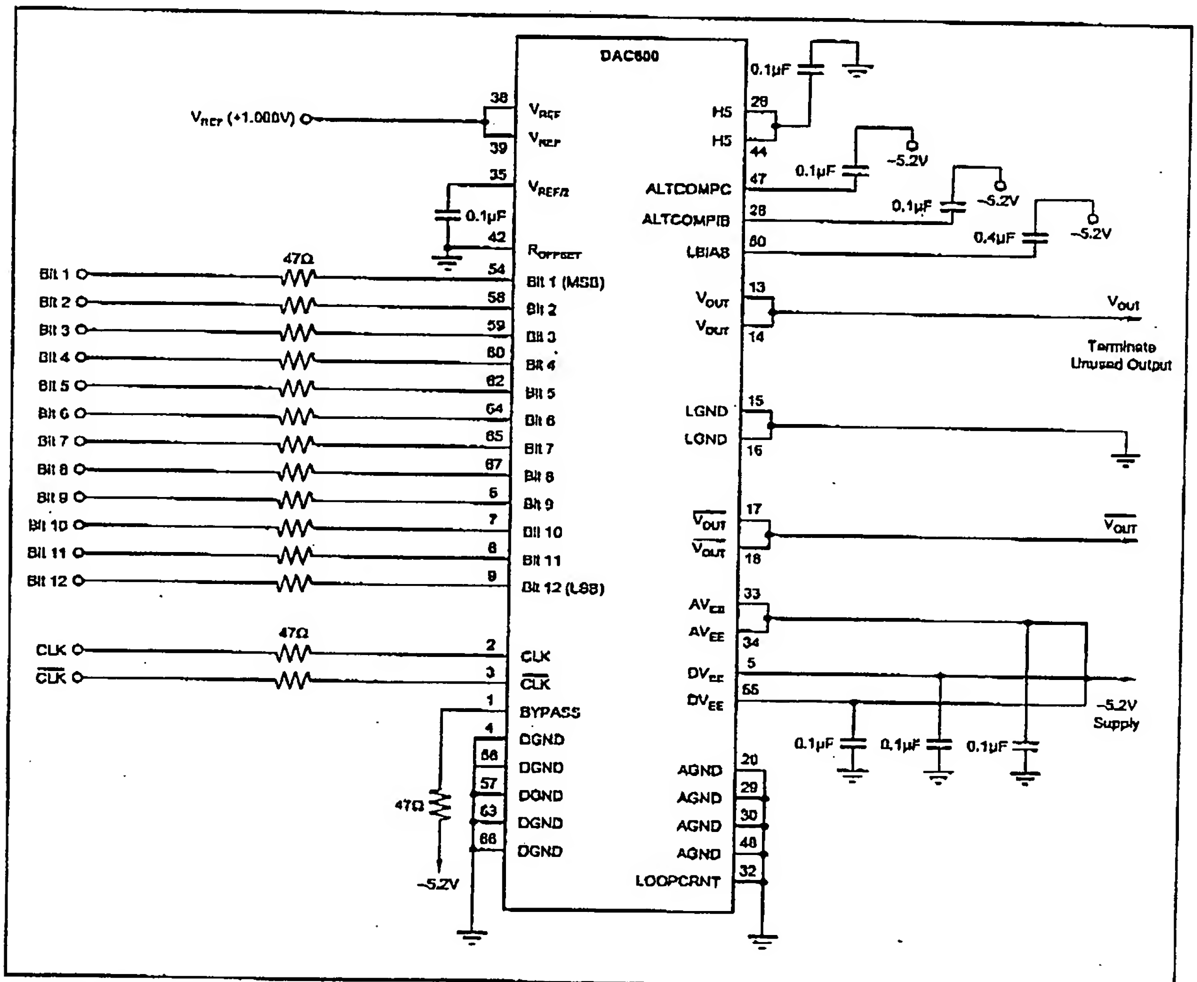


FIGURE 7. Typical DAC600 Connection Diagram.